In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) An overlay metrology mark for determining the relative position between two or more layers of an integrated circuit structure comprising a first mark portion associated with a first layer and a second mark portion associated with a second layer, wherein each mark portion comprises a two dimensional generally orthogonal array of individual test structures, wherein the overlay metrology mark does not include any additional mark portions.

2. (Previously Presented) An overlay metrology mark in accordance with claim 1 wherein each mark portion is within or on the said layer.

3. (Previously Presented) An overlay metrology mark in accordance with claim 2 wherein each mark portion is formed on the said layer by a microlithographic process.

4. (Previously Presented) An overlay metrology mark in accordance with claim 1 wherein each mark portion comprises a single two dimensional generally substantially square array of individual test structures with generally constant spacing between test structures throughout the array.

5. (Previously Presented) An overlay metrology mark in accordance with claim 1 wherein the spacing between test structures in the array comprising the first mark portion and the spacing between test structures in the array comprising the second mark portion is equivalent.

6. (Previously Presented) An overlay metrology mark in accordance with claim 5 wherein each mark portion has a generally square outline.

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7. (Previously Presented) An overlay metrology mark in accordance with claim 1 wherein each test structure has a width of around 0.5 to 2 μm.

8. (Previously Presented) An overlay metrology mark in accordance with claim 1 wherein spacing between test structures in the array is between one and four times a width of the test structure.

9. (Previously Presented) An overlay metrology mark in accordance with claim 1 wherein individual test structures of an array have substantially identically sizes and shapes and are generally square.

10. (Previously Presented) An overlay metrology mark in accordance with claim 1 wherein individual test structures comprise arrangements of design rule sized sub-structures.

11. (Previously Presented) An overlay metrology mark in accordance with claim 10 wherein the arrangements of design rule sized sub-structures are at least one of parallel arrays of elongate rectangular sub-structures in either direction, arrays of square sub-structures, circles in square or hexagonal array, arrays of holes within a suitably shaped test structure and any combinations of these or other like patterns.

12. (Previously Presented) An overlay metrology mark in accordance with claim 10 wherein sub-structures have design rule dimensions.

13. (Previously Presented) An overlay metrology mark in accordance with claim 1 wherein the arrays of test structures making up the first and second mark portions are disposed such that the first portion overlays the second portion and that the test structures of second portion are arrayed within the gaps between the test structures of the first portion and visible therebetween.

14. (Previously Presented) An overlay metrology mark in accordance with claim 13 wherein individual test structures in the second portion are located at the diagonal centre of a square bounded at each corner by test structures of the first portion.

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15. (Previously Presented) An overlay metrology mark in accordance with claim 1 wherein the test structures making up the first and second mark portions are disposed such that the first portion is laterally spaced from the second portion in a spacing direction parallel

to a horizontal or vertical direction of the square arrays such that a notional line in the spacing direction can be drawn about which each array exhibits mirror symmetry.

16. (Original) An overlay metrology mark in accordance with claim 15 wherein each mark portion comprises an identical pattern of test structures.

17. (Currently Amended) A method for providing an overlay metrology mark to determine the relative position between two or more layers of an integrated circuit structure comprises ~~the steps of~~:

laying down a first mark portion in association with a first layer;

and laying down a second mark portion in association with a second layer;

wherein each mark portion comprises a single two dimensional generally orthogonal ~~square~~ array of generally evenly spaced individual test structures and wherein no additional mark portions are laid down.

18. (Currently Amended) A method for determining the relative position between two or more layers of an integrated circuit structure, the method comprising ~~comprises the steps of~~:

laying down a first mark portion in association with a first layer;

laying down a second mark portion in association with a second layer;

wherein each mark portion comprises a single two dimensional generally ~~square~~ orthogonal array of generally evenly spaced individual test structures and wherein no additional mark portions are laid down;

optically imaging the two mark portions;

collecting and digitizing the image of the two mark portions to obtain digitized data;

numerically analysing the digitized data to obtain a quantified measurement of the misalignment of the first and second mark portions.

19. (Original) The method of claim 18 wherein optical imaging of the mark is carried out using bright field microscopy.

20. (Previously Presented) The method of claim 17 wherein individual mark portions are developed within or on the layer.

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21. (Previously Presented) The method of one of claim 17 wherein individual mark portions are formed by a microlithographic process.

22. (Cancel)

23. (Previously Presented) The method of claim 18 wherein individual mark portions are developed within or on the layer.

24. (Previously Presented) The method of claim 18 wherein individual mark portions are formed by a microlithographic process.

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